

CLAIMS

What is claimed is:

1. A graphics chip comprising:
a front-end configured to receive one or more graphics instructions and to output a geometry;
a back-end configured to receive said geometry and to process said geometry into one or more final pixels to be placed in a frame buffer;
wherein said back-end comprises multiple parallel pipelines.
2. The graphics chip of claim 1 further comprising:
a setup unit for directing said geometry into one of said multiple parallel pipelines.
3. The graphics chip of claim 2 wherein said geometry is determined to locate in a portion of an output screen defined by a tile.
4. The graphics chip of claim 1 wherein each of said parallel pipelines further comprises:
a FIFO unit for load balancing said each of said pipelines.
5. The graphics chip of claim 1 wherein each of said parallel pipelines further comprises:
a scan converter;
a rasterizer;

a unified shader; and

a texture unit.

6. The graphics chip of claim 5 wherein each of said parallel pipelines further comprises:

a z buffer logic unit; and

a color buffer logic unit.

7. The graphics chip of claim 6 wherein said z buffer logic unit interfaces with said scan converter through a hierarchical Z interface and an early Z interface.

8. The graphics chip of claim 6 wherein said z buffer logic unit interfaces with said unified shader through a late Z interface.

9. A method for processing computer graphics comprising:
receiving one or more graphics instructions in a front-end of a graphics chip and outputting a geometry;
receiving said geometry in a back-end of a graphics chip; and
processing said geometry into one or more final pixels to be placed in a frame buffer, wherein said back-end comprises multiple parallel pipelines.

10. The method of claim 9 further comprising:
using a setup unit to direct said geometry into one of said multiple parallel pipelines.

11. The method of claim 10 wherein said geometry is determined to locate in a portion of an output screen defined by a tile.

12. The method of claim 9 further comprising:
using a FIFO unit for load balancing each of said pipelines.

13. The method of claim 9 wherein each of said parallel pipelines further comprises:
a scan converter;
a rasterizer;
a unified shader; and
a texture unit.

14. The method of claim 13 wherein each of said parallel pipelines further comprises:
a z buffer logic unit; and
a color buffer logic unit.

15. The method of claim 14 wherein said z buffer logic unit interfaces with said scan converter through a hierarchical Z interface and an early Z interface.

16. The method of claim 14 wherein said z buffer logic unit interfaces with said unified shader through a late Z interface.

17. A computer program product comprising:

a computer usable medium having computer readable program code embodied therein configured to process computer graphics, said computer program product comprising:

computer readable code configured to cause a computer to receive one or more graphics instructions in a front-end of a graphics chip and output a geometry;

computer readable code configured to cause a computer to receive said geometry in a back-end of a graphics chip; and

computer readable code configured to cause a computer to process said geometry into one or more final pixels to be placed in a frame buffer,

wherein said back-end comprises multiple parallel pipelines.

18. The computer program product of claim 17 further comprises:

computer readable code configured to use a setup unit to direct said geometry into one of said multiple parallel pipelines.

19. The computer program product of claim 18 wherein said geometry is determined to locate in a portion of an output screen defined by a tile.

20. The computer program product of claim 17 wherein said computer readable code configured to cause a computer to process further comprises:

computer readable code configured to cause a computer to use a FIFO unit for load balancing each of said pipelines.

21. The computer program product of claim 17 wherein said wherein each of said parallel pipelines further comprises:

a scan converter;

a rasterizer;
a unified shader; and
a texture unit.

22. The computer program product of claim 21 wherein each of said parallel pipelines further comprises:

a z buffer logic unit; and
a color buffer logic unit.

23. The computer program product of claim 22 wherein said z buffer logic unit interfaces with said scan converter through a hierarchical Z interface and an early Z interface.

24. The computer program product of claim 22 wherein said z buffer logic unit interfaces with said unified shader through a late Z interface.